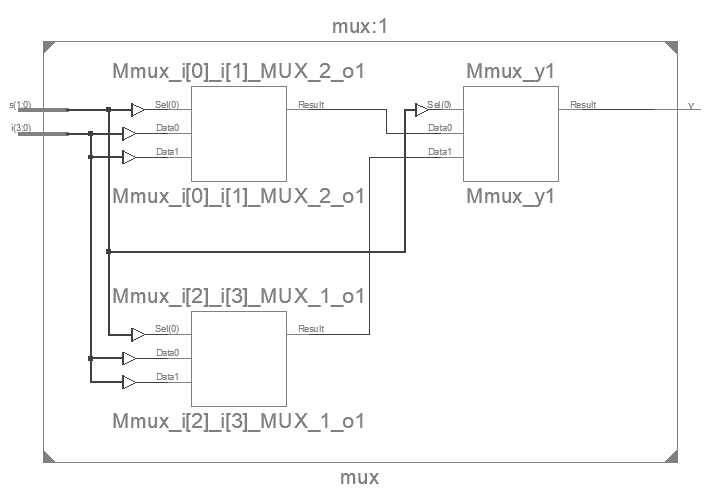
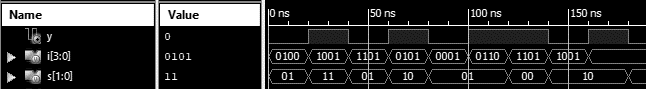
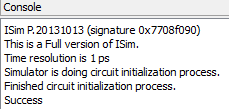
**RTL Diagram:**

****

**Output Waveform:**

****

**Simulation Output:**

****

**Experiment-1**

**Objective:**

To design a 4x1 Multiplexer and write a simple test bench for it. The test bench should generate stimulus to completely verify the functionality of the design under test with delay of 20ns.

**Theory:**

Multiplexer is a combinational circuit that has maximum of 2n data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines such that, each combination will select only one data input.

**Design Code:**

module mux(input [3:0]i, [1:0]s, output y);

    assign y = s[1]?(s[0]?i[3]:i[2]):(s[0]?i[1]:i[0]);

endmodule

**Testbench Code:**

module mux\_tb;

    reg [3:0] i;

    reg [1:0] s;

    wire y;

    integer x = 0;

    mux uut(i,s,y);

    initial begin

        repeat(10)begin

            i = $random;

            s = $random;

            #20;

            if (y != i[s]) x = x + 1;

        end

        if(!x) $display("Success");

        else $display("Failure");

    end

endmodule

**Result:**

The simulation output and the RTL diagram is observed and found to be valid.